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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,395	12/30/2003	Vasudevan Srinivasan	42P18068	8966

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EXAMINER	
KENDALL, CHUCK O	

ART UNIT	PAPER NUMBER
2192	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,395	SRINIVASAN ET AL.	
	Examiner	Art Unit	
	Chuck O. Kendall	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/23/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

1. This is in response to the application filed on 04/23/07.

2. Claims 1, 2, 4 – 22 and 24 - 27 have amended.

Claim Rejections - 35 USC § 102

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1, 2, 4, 5, 20 – 22 and 24 are rejected under 35 U.S.C. 102(e) as being unpatentable over Asai et al. US 5,903,730.

Regarding claims 1,18 and 21, Asai discloses a method, and machine accessible medium and system comprising:

determining processor utilization in a data processing system (FIG. 11, and all associated text and

synchronizing execution of a plurality of threads in the data processing system to prevent interrupting the determining of the processor utilization (4:45 – 50) and using one of a plurality of logical processors in the data processing system (3:25 – 30, discloses three in parallel and running together, which is consistent with Applicants definition of logical processor in paragraph [0022] of Applicant's specification).

Regarding claims 2,19 and 22, the method of claim 1, further including processing the plurality of threads simultaneously on a plurality of logical processors (4:45 – 50, see parallel processing).

Regarding claims 4 and 24, the method of claim 2, wherein the synchronizing further includes executing a predetermined unit of code on the plurality of logical processors, except the one determining the processor utilization, to prevent interrupting the determining of the processor utilization (Asai, FIG. 8, see S15a and S15e).

Regarding claims 5 and 20, the method of claim 4, wherein determining the processor utilization comprises calculating a frequency of the one of the plurality of logical processors (Asai, FIG. 15e, see calculating the execution time of each parallel).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6 – 17 and 25 – 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asai et al. US 5,903,730 in view of Horst USPN 5,384,906.

Regarding claim 6 and 25, the method comprising:

determining processor utilization in a data processing system having a plurality of physical processors(Asai, 2:7 – 10, shows a plurality of routines, each thread here would equivalent to a routine);

processing a plurality of threads simultaneously on the plurality of physical processors (Asai, 4:45 – 50, see parallel processing);

and synchronizing execution of the plurality of threads in a data processing system to prevent interrupting the determining of the processor utilization (3:25 – 30, discloses three in parallel and running together, which is consistent with Applicants definition of logical processor in paragraph [0022] of Applicant's specification and 4:45 – 50).

Asai doesn't expressly disclose pausing execution of the plurality of threads during the determining of the processor utilization

However, Horst in an analogous art and similar configuration discloses the halting of processor instructions in its respective instruction stream and being able to determine event counts (37:9 – 20). Therefore it would have been obvious to one of ordinary skill in the art to combine Asai and Horst, because it would enable comparing each of the other CPU's and determine the event counts as suggested by Horst.

Regarding claims 7 and 26, the method of claim 6, wherein the determining includes one of the plurality of physical processors determining the processor utilization (FIG. 11, s18a – i, and all associated text).

Regarding claims 8 and 27, the method of claim 7, wherein synchronizing the execution of the plurality of threads comprises executing a predetermined unit of code

on the plurality of physical processors, except the one determining the processor utilization, to prevent interrupting the determining of the processor utilization (FIG. 8, see S15a and S15e).

Regarding claim 9, the method of claim 8, wherein determining the processor utilization comprises calculating a frequency of the one of the plurality of physical processors (FIG. 15e, see calculating the execution time of each parallel).

Regarding claim 10, Asai discloses method comprising:

determining processor utilization in a system executing at least a first thread and a second thread (Asai, 2:7 – 10, shows a plurality of routines, each thread here would equivalent to a routine).

Asai doesn't expressly disclose pausing execution of the second thread during the determining of the processor utilization.

However, Horst in an analogous art and similar configuration discloses the halting of processor instructions in its respective instruction stream and being able to determine event counts (37:9 – 20). Therefore it would have been obvious to one of ordinary skill in the art to combine Asai and Horst, because it would enable comparing each of the other CPU's and determine the event counts as suggested by Horst.

Regarding claim 11, the method of claim 10, further comprising executing at least the first and the second threads simultaneously on at least a first processor and a second processor in the system (Asai, 4:45 – 50, see parallel processing).

Regarding claim 12, the method of claim 10, the determining including the first processor determining the processor utilization (Asai, 4:7 – 15, see analyzing contents and profile information, also see FIG. 11 and all associated text).

Regarding claim 13, Asai discloses an apparatus comprising:

a plurality of processors, one of the plurality of processors to determine processor utilization and the remaining processors to execute a predetermined unit of code to prevent interrupting the one determining the processor utilization (FIG. 11, and all associated text). Asai doesn't expressly disclose a bus coupling the plurality of processors to each other.

However, Horst in an analogous art and similar configuration discloses, "External interrupts are synchronized among the three CPUs by a technique employing a set of busses 18 for coupling the interrupt requests and status from each of the processors to the other two" (9:52 – 57).

Therefore it would have been obvious to one of ordinary skill in the art to combine Asai and Horst because it would enable synchronizing the external interrupts and provide status of each of the processors as suggested by Horst.

Regarding claim 14, the apparatus of 13, further comprising a performance monitor counter coupled to each of the plurality of processors to keep track of when the processor is active (Asai, FIG. 11).

Regarding claim 15, the apparatus of 14, the performance monitor counter to provide a count for determining the processor utilization (Asai, 8:32 – 36).

Regarding claim 16, the apparatus of claim 13, wherein the plurality of processors comprise a plurality of logical processors to execute threads simultaneously (Asai, FIG.1, 12a – 12c).

Regarding claim 17, Asai as applied in claim 13 pausing the remaining processors (Horst, 37:9 – 20).

Response to Arguments

7. Applicant's arguments with respect to claims 1 – 27 have been considered but are moot in view of the new ground(s) of rejection.

With regards to the limitation of "using one of a plurality of logical processors in the data processing system" in claim 1, Examiner believes that Asai the prior art of record still discloses this limitation see (3:25 – 30), which is consistent with Applicants definition of logical processor in paragraph [0022] of Applicant's specification. The rejection above in claim 1 addresses this limitation.

Correspondence information

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuck Kendall whose telephone number is 571-272-3698. The examiner can normally be reached on 10:00 am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ck.

TUAN DAM
SUPERVISORY PATENT EXAMINER